IN THE SPECIFICATION

Please replace the paragraph at page 9, lines 6-17, with the following rewritten paragraph:

Here, a first delivery stage 24 is provided at carrier block B1 in the vicinity of the region connected to transfer block B2, for delivering wafer W between first transfer means 22 of carrier block B1 and second transfer means 23 of transfer block B2. This delivery stage 24 is configured, e.g., in two stages of: a delivery stage for loading, for use in loading wafer W to transfer block B2; and a delivery stage for unloading, for use in unloading wafer W ~~to~~ from transfer block B2. It is noted that delivery stage 24 may be provided in transfer block B2 in a region accessible by first transfer means 22. Alternatively, it may be configured in one stage so that a common delivery stage can be used for loading/unloading wafer W with respect to transfer block B2. For example, the delivery stage has a structure capable of supporting three substrates at the back surfaces, and is configured not to interfere with the respective arms of first and second transfer means 22 and 23.

Please replace the paragraph at page 10, line 20 to page 11, line 7, with the following rewritten paragraph:

Shelf units U2, U3 are each configured by stacking a plurality of units at the region accessible by second transfer means 23 of transfer block B2. In this example, there are provided for example three vacuum drying units (VD) for removing solvent included in the coating solution after the liquid processing performed at the coating unit, the anti-reflection coating forming unit and the like, for example four heating units (LHP) for use in prescribed heating processing of wafer W before coating with the resist solution or for use in heating processing after development, for example one heating unit (PAB), called a pre-baking unit or the like, for performing heating processing on the wafer after coating with the resist

solution, for example two heating units (PEB), called a post-exposure baking unit or the like, for performing heating processing on the wafer W after exposure to light, for example three temperature regulating units (CPL) that are units for adjusting wafer W to a prescribed temperature, a hydrophobic process unit (ADH) for performing hydrophobic processing on the wafer surface, and additionally, for example one delivery unit (TRS1) for loading wafer W to process block B3, and for example one delivery unit (TRS2) for unloading wafer W from process block ~~S1~~ B3, which are allocated in a vertical direction.

Please replace the paragraph at page 11, lines 8-17, with the following rewritten paragraph:

Delivery units ~~TRA1~~ TRS1, TRS2 correspond to the second delivery stage of the present invention. Although Figs. 3-5 show an example of the layout of these units, the number and the types of the units are not limited thereto, and in this example as well, it may be configured to have a single delivery unit to be used for both loading of wafer W to process block B3 and unloading of wafer W from process block B3. Further, the delivery unit (TRS2) may be added with a temperature regulating function for the purpose of lowering the temperature of the wafer, and it may be configured such that this temperature regulating function is used to lower the temperature of wafer W when delivering the same after the processing in the heating unit (PAB), or after the heating processing following the developing processing, for example.

Please replace the paragraph at page 13, lines 5-11, with the following rewritten paragraph:

Hereinafter, configurations of coating-related unit 32, the heating unit (PEB) and others provided at process blocks ~~B3, B4~~ B3-B5 will be described in brief. Firstly, coating-

related unit 32 such as the coating unit or the anti-reflection coating forming unit is described with reference to Fig. 6. Although the coating-related unit used may have a configuration of a spin coating type where a processing solution is supplied onto the substrate and spread by rotation as will be described later, herein, a scanning coating device is described by way of example.

Please replace the paragraph at page 20, line 12 to page 21, line 3, with the following rewritten paragraph:

In the case where the wafer within carrier C is wafer WA to be subjected to the first processing, when the process block to which the relevant wafer WA is to be transferred is determined to be first process block B3, for example, the process recipe of wafer WA is transmitted from system control portion 81 to process block control portion 82A of the relevant process block B3. As described above, in process block control portion 82A, the process units for use are selected based on the process recipe, and processing is performed in each of the process units under predetermined processing conditions. More specifically, in the first processing, wafer WA firstly carried in via delivery unit TRS1 is transferred in the order of a temperature regulating unit (CPL) → a coating-related unit (COT) for formation of the anti-reflection coating on the lower-layer side → heating unit (LHP) or a vacuum drying unit (VD) → temperature regulating unit (CPL) → coating unit (COT) → heating unit (PAB) or vacuum drying unit (VD) → temperature regulating unit (CPL) → an upper-layer anti-reflection coating forming unit (COT) → heating unit (LHP) or vacuum drying unit (VD), during which the anti-reflection coating on the lower-layer side (Bottom-ARC), the film of the resist solution, and the anti-reflection coating on the upper-layer side (Top-ARC) are formed in this order from the lower side, and then carried out via delivery unit TRS2 to be subjected to light exposure processing at light exposure device B7. Here, the next step of that

of ~~coating liquid~~ coating-related unit (COT) may be performed using either heating unit (LHP, PAB) of hot plate type or vacuum drying unit (VD).

Please replace the paragraph at page 21, lines 4-14, with the following rewritten paragraph:

Next, wafer WA having been exposed to light is transferred through the above-described path to the original process block ~~S1~~ B3 where the resist solution was applied, via a delivery unit TRS1 for use in input of the relevant process block. It is transferred through heating unit (PEB) → temperature regulating unit (CPL) → developing unit (DEV), where predetermined developing processing is performed. It is then adjusted to a predetermined temperature in heating unit (LHP), and carried out via delivery unit TRS2. The first processing for forming the lower-layer anti-reflection coating, the resist film and the upper-layer anti-reflection coating is carried out in this manner. Thus, in the process block to which wafer WA to be subjected to the first processing is transferred, the above-described process units are selected, and predetermined processing is carried out in each process unit.

Please replace the paragraph at page 22, line 25 to page 23, line 4, with the following rewritten paragraph:

Next, wafer [[W]] WC having been exposed to light is transferred to process block B5 where application of the resist solution and formation of the lower-layer anti-reflection coating were performed, through the path similar to those in the first and second processing described above, to be subjected to predetermined developing processing. The lower-layer anti-reflection coating and the resist film are formed in this manner. As such, in process block B5 to which wafer WC to be subjected to the third processing is transferred, the above-

described process units are selected, and predetermined processing is carried out in each of the process units.

Please replace the paragraph at page 23, lines 9-18, with the following rewritten paragraph:

In this configuration, transfer block B2 is provided, and second transfer means 23 of the relevant transfer block B2 performs delivery of wafers W between carrier block B1 and respective process blocks B3-B5, and between respective process blocks ~~B3-B4~~B3-B5 and interface portion B6. Further, in the respective process blocks B3-B5, parallel processing is carried out for each block. This means that third transfer means 31 of each process block B3-B5 only needs to take charge of transfer of wafer W within the relevant process block B3-B5, so that the burden of transfer means 31 is alleviated compared to the conventional case. As such, it is less probable that transfer of processed wafer W by transfer means 31 is awaited, which leads to reduction in transfer time and, hence, improvement in throughput when seen as the entire apparatus.

Please replace the paragraph at page 29, lines 5-16, with the following rewritten paragraph:

In the example shown in ~~Fig. 15~~ Figs. 15A and 15B, a shelf unit U7 provided with a peripheral light exposure device (WEE), a buffer cassette (BUF), a temperature regulating unit (CPL), and a heating unit (PEB) is arranged between delivery means 26 and sub-transfer arm [[93]] 96. Wafer W is transferred by delivery means 26 in the order of, e.g., delivery stage 27 → peripheral light exposure device (WEE) → buffer cassette (BUF) → temperature regulating unit (CPL). Thereafter, wafer W of temperature regulating unit (CPL) is transferred by sub-transfer arm 96 in the order of light exposure device B7 → heating unit

(PEB), and then, wafer W in heating unit (PEB) is transferred again by delivery means 26 in the order of buffer cassette (BUF) → delivery stage 27. Further, it may be configured such that the peripheral light exposure device is not provided. In this case as well, wafer W is transferred in a similar manner as described above, except that processing with the peripheral light exposure device is not conducted.

Please cancel the original Abstract at page 38, lines 1-14 in its entirety, and insert therefor the following replacement Abstract on a separate sheet as follows: